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REMARKS: ☐ Urgent ☐ For your review ☐ Reply ASAP ☐ Please comment

Ser. No. 10/711,151 Group 2816 Docket PS-125

DRAFT DRAFT

Attached is a draft of my proposed claim amendments for claims 1-3. I approve your proposed amendments of claims 9 and 15 and would also approve an examiners amendment with the attached edits to claims 1-3.

Thank You.

I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office.

Signed _____ /Stuart T Auvinen/ _____
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Date Signed and transmitted _____11/14/05_____

1. A charge pump comprising:

an up input and a down input to the charge pump;

an output having an output capacitance to be charged in response to the up input and discharged in response to the down input;

a fixed current source that sources a relatively constant source current to a first junction node;

a variable current source that sources a varying source current to a second junction node, wherein the varying source current varies in response to a control voltage;

a first driver transistor, coupled to conduct current between the first junction node and the output in response to the up input;

a second driver transistor, coupled to conduct current between the second junction node and the output in response to the down input;

a first series transistor, coupled to conduct current between the first junction node and an intermediate node in response to ~~an inverse of~~ the up input being inactive;

a second series transistor, coupled to conduct current between the second junction node and the intermediate node in response to ~~an inverse of~~ the down input being inactive;

a sampling capacitor for storing a sampled charge, generating the control voltage to the variable current source; and

a sampling switch coupled to conduct current between the intermediate node and the sampling capacitor when the up input and the down input are inactive,

whereby the intermediate node is coupled to the sampling capacitor to adjust the varying source current.

2. The charge pump of claim 1 wherein the sampling switch comprises a sampling transistor and a logic gate;

wherein the sampling transistor receives a logic output signal on a gate;

wherein the logic gate receives the up input and the down input or an ~~the~~ inverse of the up input and ~~the~~ an inverse of the down input and generates the logic output signal.

3. The charge pump of claim 1 wherein the sampling switch comprises a first sampling transistor and a second sampling transistor in series between the intermediate node and a control node of the sampling capacitor;

wherein the first sampling transistor receives ~~the~~ an inverse of the up input on a gate;

wherein the second sampling transistor receives ~~the~~ an inverse of the down input on a gate.